Patent Claims

1. Method of caching commands in microprocessors having a plurality of arithmetic units and in modules having a two- or multidimensional cell arrangement (e.g. FPGAs, DPGAs, DFPs or the like), characterized in that

1.1 a plurality of cells and arithmetic units (CEL) are combined to form a plurality of groups, a cache unit (CT) being assigned to each subgroup;

1.2 the cache units of the individual subgroups are connected, via a tree structure, to a higher level cache unit (ROOT CT) having access to the command memory memory [sic] (ECR) in which the commands are stored;

1.3 commands are combined to form command sequences (KR), which are always cached as a whole and transmitted between the caches;

1.4 each cache unit on the lowermost or middle level of the tree requests the required commands from the respectively assigned higher level cache unit;

1.5 a higher level cache unit sends a requested command sequence to the lower level unit if it holds the command sequences in its local memory;

1.6 a higher level cache unit requests a requested command sequence from the respective higher level cache unit if it does not hold the command sequences in its local memory;

2. Method according to Claim 1, characterized in that command sequences are deleted as a whole.

3. Method according to Claims 1 through 2, characterized in that command sequences of a cache unit are deleted if there is insufficient room in the local memory for loading an additional requested command sequence.

4. Method according to Claims 1 through 2, characterized in that a command (REMOVE) within a command sequence triggers an action through which the command sequences of a cache unit are deleted.

5. Method according to Claims 1 through 4, characterized in that a command (EXECUTE) within a command sequence triggers the loading of a certain complete command sequence.

6. Method according to Claims 1 through 5, characterized in that any desired command (EXECUTE, REMOVE, etc.) via a bus link between the cache units triggers an action on any desired addressed cache unit according to the command.

7. Method according to Claims 1 through 6, characterized in that a program sequence that is not effectively cachable because it is only used by one cache unit, is broken into small subsequences which are needed by a plurality of cache units, an additional subsequence (IKR) contains the non-cachable remainder of the command sequence and the calls of the cachable subsequences.

7. Method according to Claims 1 through 6, characterized in that statistics providing information concerning the age of the command sequence, i.e., the dwelling time in the memory of the cache unit, are assigned to each command sequence.

8. Method according to Claims 1 through 6, characterized in that statistics providing information concerning the frequency of the calls of the command sequence are assigned to each command sequence.

9. Method according to Claims 1 through 6, characterized in that statistics providing information concerning the length of the command sequence are assigned to each command sequence.

10. Method according to Claims 1 through 9, characterized in

that the delete routine is designed so that it evaluates the statistics of each command sequence and removes the least significant command sequence according to the algorithm executed.

11. Method according to Claims 1 through 10, characterized in that the delete routine can be adjusted to the algorithm to be executed in a programmable manner.